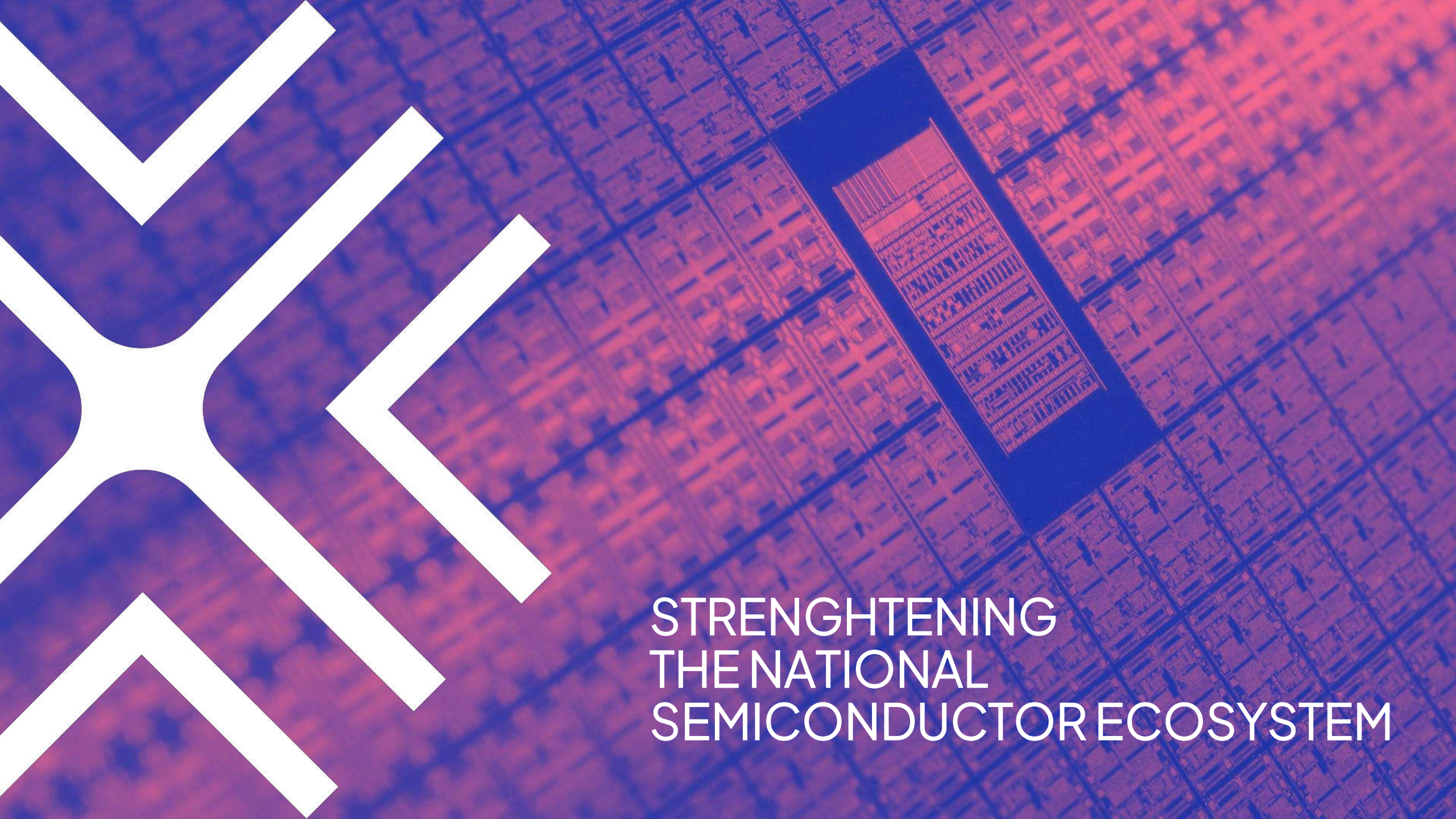

Chips-IT


STRENGHTENING
THE NATIONAL
SEMICONDUCTOR ECOSYSTEM

WHAT IS CHIPS-IT

CENTRO ITALIANO PER IL DESIGN DEI CIRCUITI INTEGRATI A SEMICONDUTTORE

Private Foundation
entity type

€ 20 M/y
research budget

€ 3.8 M/y
admin budget

Ministero delle Imprese e del Made in Italy

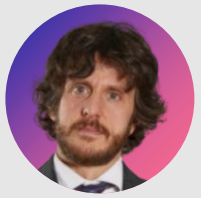
Ministero dell'Economia e delle Finanze

SUPERVISORY BOARD

Prof. Alberto Sangiovanni-Vincentelli
President

Prof. Enrico Sangiorgi
MEF

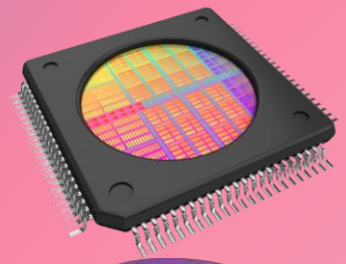
Prof. Francesco Svelto
MUR



Marco Calabrò
MIMIT

IDEA

PROOF



PRODUCT

Univertsities &
Research Centers

Chips-IT

LEs

SMEs

Start-ups

FRONTIER RESEARCH

INDUSTRIAL RESEARCH

COMMERCIALIZATION

SCIENTIFIC COMMITTE

MARIAN VERHELST
KU Levuen

CLARK T.C.NGUYEN
University of California at Berkeley

ALESSANDRO CREMONESI
ST Microelectronics

ERNESTO LASALANDRA
Ferrari

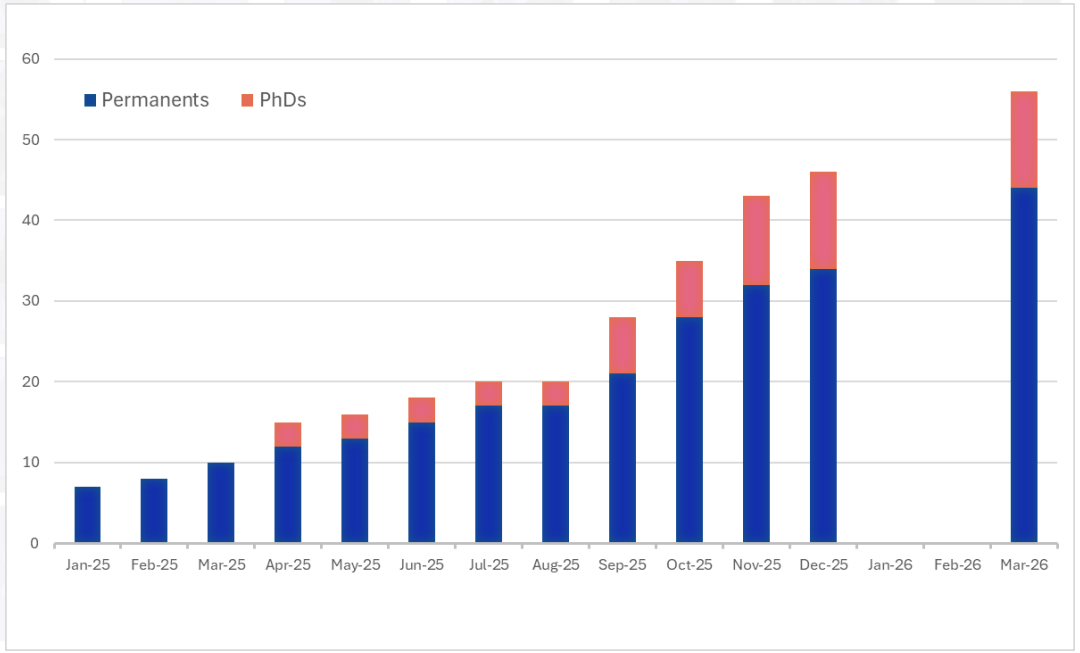
RINALDO CASTELLO
University of Pavia

SUBASISH MITRA
Stanford University

ANGELO CASERO
Leonardo

WHERE ARE WE?

OUR PATH



Headcount

59 people

4 managers

7 administrative & staff

33 super researchers

3 external collaborators

12 PhD fellows

Gender

83% **17%**

Cursus

100%
5 years degree

12
permanents with PhD

Age

research lines only

33
average

56
oldest

22
youngest

Locations

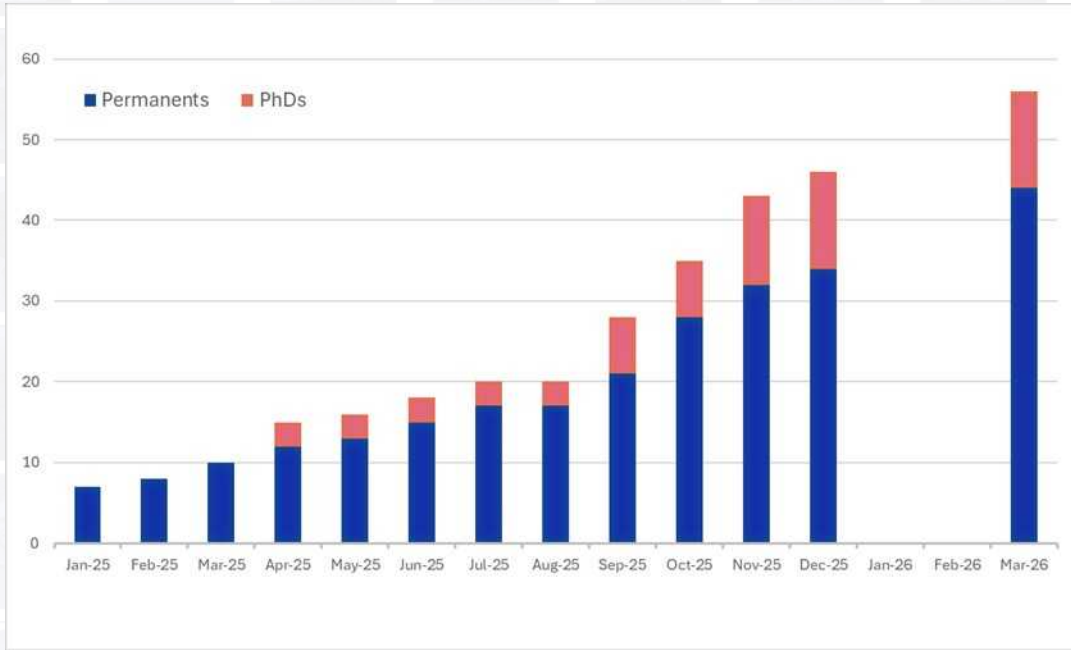
Pavia
Headquarter

Bologna
Second site

Tape-out

4 completed

3 in preparation



Publications

7 published

1 accepted

3 submitted

Conferences

3 Invited talks

7 oral participation

WHERE ARE WE?

FUNDED PROJECTS

EU Chip Design Platform

Coordinator	**IMEC**
Funding % of total cost	€ 2.2M 100%
Started Ends	01/01/25 31/12/28

Support startups & SMEs to access everything needed to design and launch microchips

Chip Competence Center

Coordinator	**Chips-IT**
Funding % of total cost	€ 2.1M 50%
Starting Ends	01/01/26 31/12/29

National reference point for Europe for the semiconductor sector.

Wide BandGap pilot line

Coordinator	**CNR**
Funding % of total cost	€ 2.0M 100%
Started Ends	01/06/25 30/05/29

Pilot line for the development, of energy efficient wide bandgap semiconductors

CHASSIS

Coordinator	**Bosch**
Funding % of total cost	€ 0.1M 35%
Starting Ends	01/11/25 31/10/28

Heterogeneous integration for automotive high-performance computing.

TURANDOT

Coordinator	**NXP**
Funding % of total cost	€ 2.4M 70%
Started Ends	TBD TBD

Developmet of RISC-V processors for automotive

WHERE ARE WE?

UNIVERSITIES AND RESEARCH INSTITUTES

Framework Agreement
location and renovations for Chips-IT @ PTS

UNIVERSITÀ DI PAVIA

MoU
joint projects on chip design & HPC

CINECA ICSC Centro Nazionale di Ricerca in HPC, Big Data and Quantum Computing

MoU
new location for Chips-IT @ DAMA Tecnopolo

RegioneEmiliaRomagna

Framework Agreement
Silicon development for robotics and Human-Brain Interfaces (set-up phase)

Framework Agreement
Cooperation and PhD sponsoring (2) Engineering

Framework Agreement
Cooperation and PhD sponsoring (5) Engineering & Economy

INDUSTRY AND ECOSYSTEM ENGAGEMENT

Chips-IT

life.augmented

LEONARDO

Participation to the Scientific Committee

28+

NDAs and MoUs

signed with corporates, SMEs, VCs and local development hubs.

4

Projects

Submitted partnering with industry. Two successful with Stellantis and ST Microelectronics.

1

request to become **Participating Member**

Chips-IT will support EssilorLuxottica on its new journey as a fabless IC company, co-developing the next generation of ASICs for smart eyewear

EssilorLuxottica

Chips-IT

CHIPS-IT OBJECTIVES

CONTEXT: Europe & Italy

Europe below its economic weight

Semiconductor share lags Europe's economy in both volume and value, especially in consumer and high-end market

Structural, slow decline

Decline cannot be reversed quickly; focusing only on production is not enough – action is needed at the system integration level

Italy: broad but thin supply chain

Components and system integrations are contentrated in

Automotive | Industrial | Aerospace

value chain is broad, but capabilities are thin and fragmented

STRATEGIC OBJECTIVES

1 Performing excellent research

Establishing Italy as a contributor, not a follower, in IC design knowledge and innovation.

2 Strengthening the ecosystem

Consolidating a fragmented national landscape into a coherent, high-functioning semiconductor community.

3 European reference

Ensuring alignment with, and influence within, major communitarian and Chips Act programmes.

4 Reduce the talent gap

Building a sustainable pipeline of designers, researchers, entrepreneurs and innovators for Italy and Europe.

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TECHNICAL OBJECTIVES

1 AI Introduction

Addressing the introduction of AI passing from chips for autonomous systems to near edge and progressively to HPC

2 Interface

Optimizing the interface between the physical world and the AI/computing functions for performing autonomous systems

3 Transmission

Develop future transmission systems through high component integration allow by components miniaturization and frequency increase

4 Power efficiency

Address the challenge of power supplying in systems where the power density is continuously increasing

Chips-IT Research Branch

DIGITAL DESIGN & OPEN HARDWARE

- RISC-V, Edge computing, Open source EDA tools

ANALOG & M/S PROCESSING

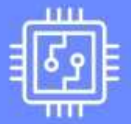
- High performance sensor interfaces and processing

RADIO FREQUENCY TO TERAHEARTZ

- Phased array, Beamforming 3D antenna, mmWave

POWER ICs AND DEVICES

- Energy conversion, ICs converters



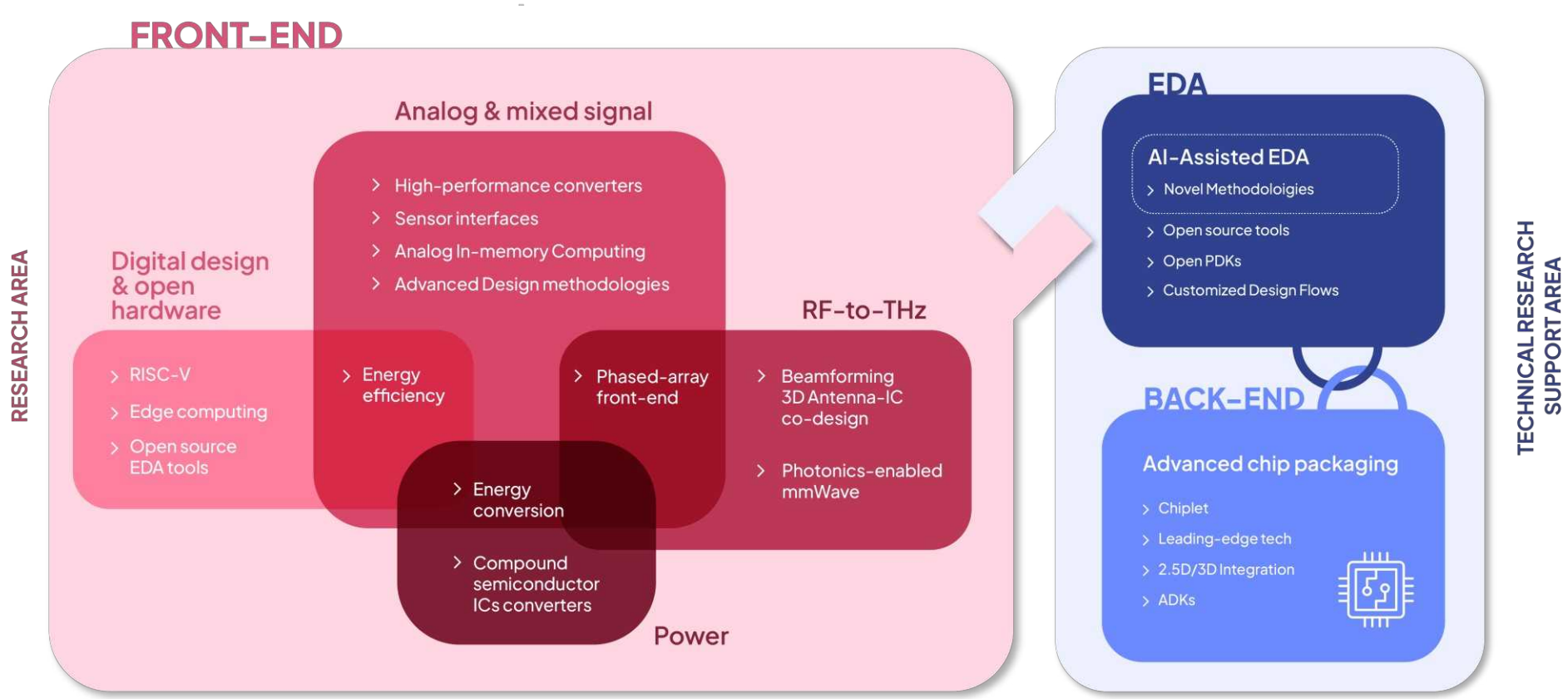
ADVANCED CHIP PACKAGING

- Chiplet, Leading-edge tech, ADKs

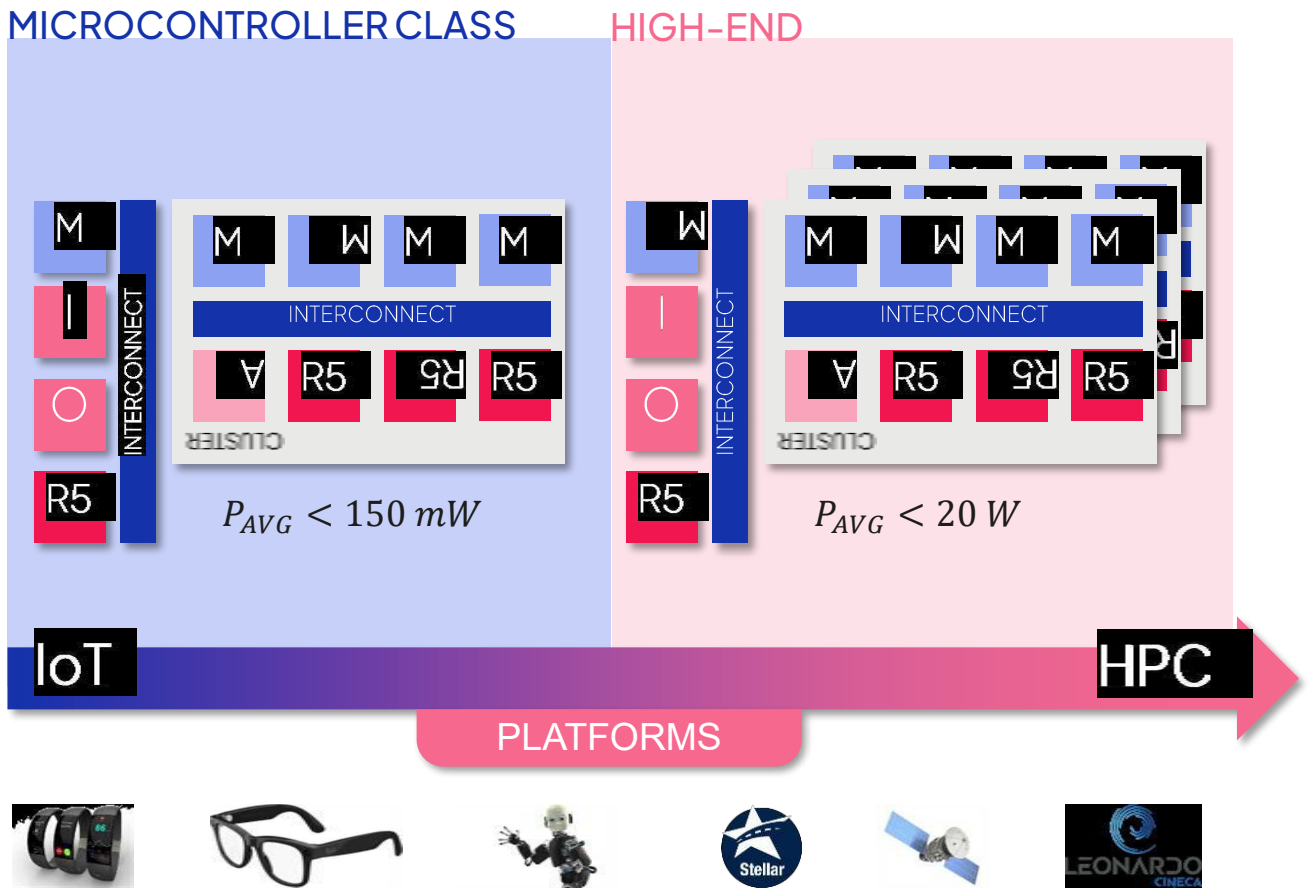
INFRASTRUCTURE & AI-ASSISTED EDA

- Emulation, EDA, Characterization lab

SCIENTIFIC PLAN

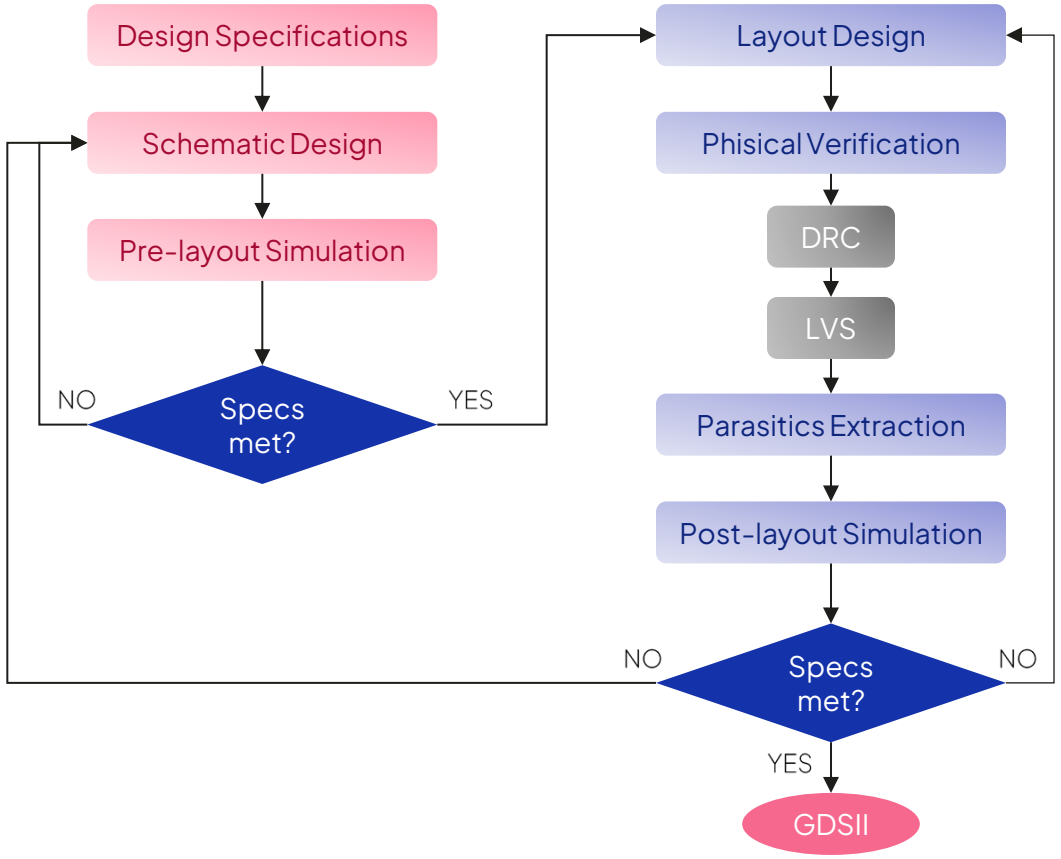


DIGITAL DESIGN & OPEN HARDWARE



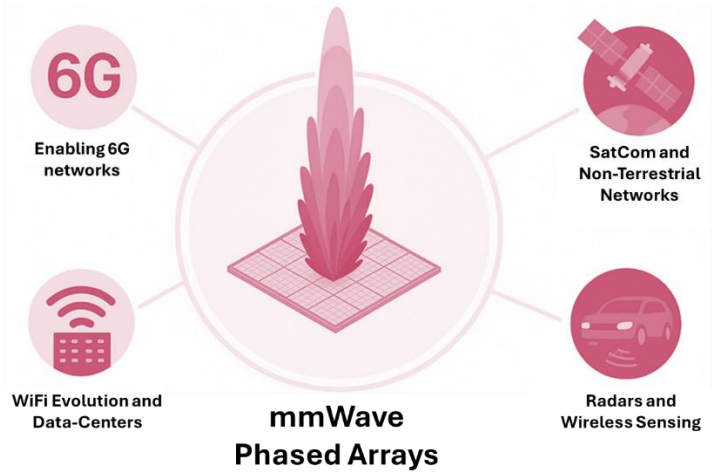
- Targeting high energy efficient systems for Aerospace, Robotics and Automotive
- IoT SoCs for edge-AI: near sensor processing, Wearable Devices, HMIs
- High Performance SoCs: HPC, Data analysis and ML, LLM training and Inference, Life Science
- Developing IP cores and accelerators, building on top of the RISC-V ISA based PULP platform
- Targeting independence from commercial IP
- Strong verification activities and HW/FW/SW co-development thanks to hardware emulator infrastructure

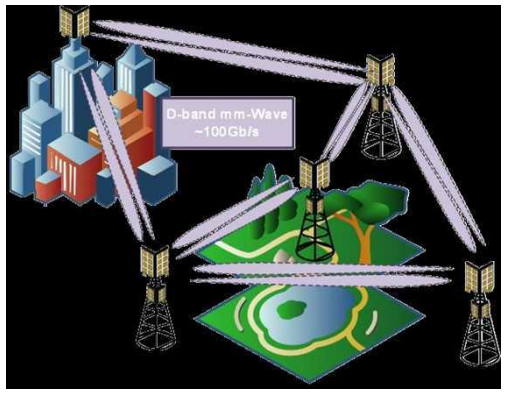
ANALOG & MIXED SIGNAL

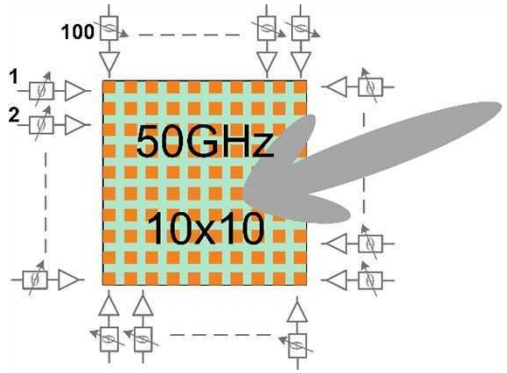


- Fundamental in the overall strategy as it is central to manage the interface to the physical reality
- Diversified and wide ranging in applications
- Strong expertise in Italy and in Pavia area in particular
- High potential impact on Start-Ups and SMEs
- Only group not built on a pre-existing academic lab, requiring a longer time to reach effectiveness and strategic partners

RF-to-THz







- Innovating in highly-integrated MIMO and phased-array transceivers for terrestrial and space communications
- Enabling Tbps interconnects with unprecedented efficiency
- Benchmarking of silicon and compound semiconductor technologies for mmWave & SubTHz Ics
- Development of critical components addressing the demanding performance and efficiency of future applications
- Setting up and leveraging on a state-of-the-art test infrastructure

INFRASTRUCTURE

Designing, simulating and taping-out

Server to run EDA tools in a secure environment and on industry standards

Emulating and verifying

The first emulator physically in Italy to perform industry level verification and hardware/software co-design

Assembling

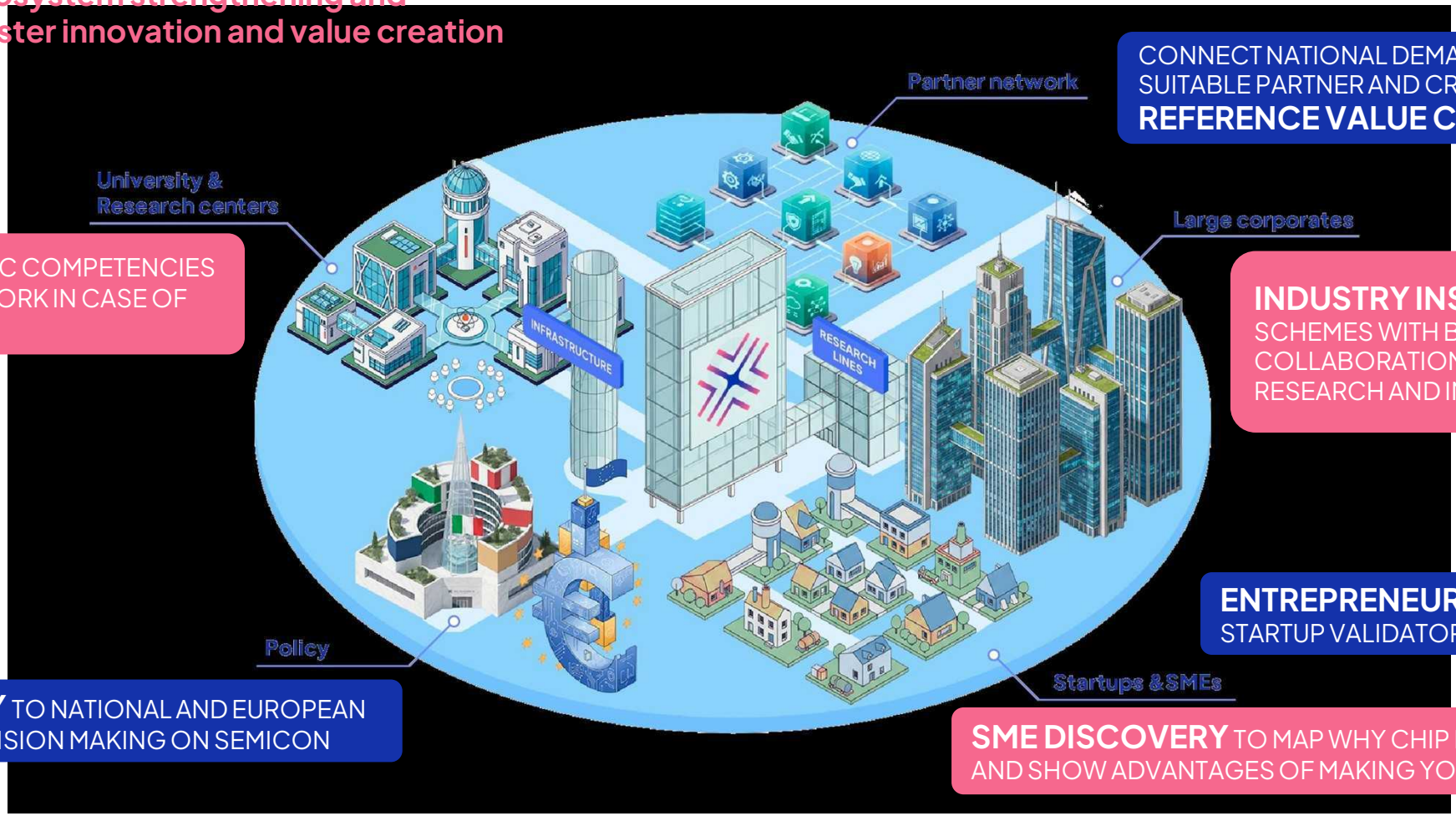
On premise and co-investing with other institutes to have basic and mid-range assembly capability for testing and validation

Testing and validating

Top performance dedicated high end testing equipment for RF, digital and analog circuits

BUILDING AN ECOSYSTEM

Semiconductor ecosystem strengthening and orchestration to foster innovation and value creation



CONNECT NATIONAL DEMAND WITH THE MOST SUITABLE PARTNER AND CREATE A **REFERENCE VALUE CHAIN**

MAPPING ACADEMIC COMPETENCIES TO EFFICIENTLY NETWORK IN CASE OF INDUSTRY DEMAND

INDUSTRY INSPIRED COOPERATION SCHEMES WITH BALANCED ENGINEERING COLLABORATION BETWEEN ACADEMIA, RESEARCH AND INDUSTRY

ENTREPRENEURIAL SUPPORT AND STARTUP VALIDATOR GATEWAY TO VCs

GATEWAY TO NATIONAL AND EUROPEAN POLICY DECISION MAKING ON SEMICON

SME DISCOVERY TO MAP WHY CHIP DESIGN IS A TABOO AND SHOW ADVANTAGES OF MAKING YOUR OWN CHIP

TECHNOLOGY TRANSFER

Pillar 1

- Industrial-relevant, roadmap-driven collaborations
- Mid-to-high TRL co-design projects
- Outputs become silicon-validated assets

Pillar 2

- Professional backbone for IP management
- Enables predictable technology adoption
- Enforces early IP identification methodologies

Pillar 3

- Forming entrepreneurial minds and actively supporting them
- Safe space for startups and unfounded teams
- Best place to be for a semiconductor startup in Italy

INFRASTRUCTURE INVESTMENT PLAN

Designing, simulating and taping-out

2026
Completion existing rack
2M€

2028
Further expansion
3M€

Emulating and verifying

Early 2026
2.5Billion gates system
10M€

Early 2027
2.5Billion gates addition
10M€

Assembling

Early 2026
Initial capability on premise in Pavia
3M€

Early 2027
Added capability in Pavia or co-investing with partner
3M€

Early 2028
Added capability in Pavia or co-investing with partner
7M€

Testing and validating

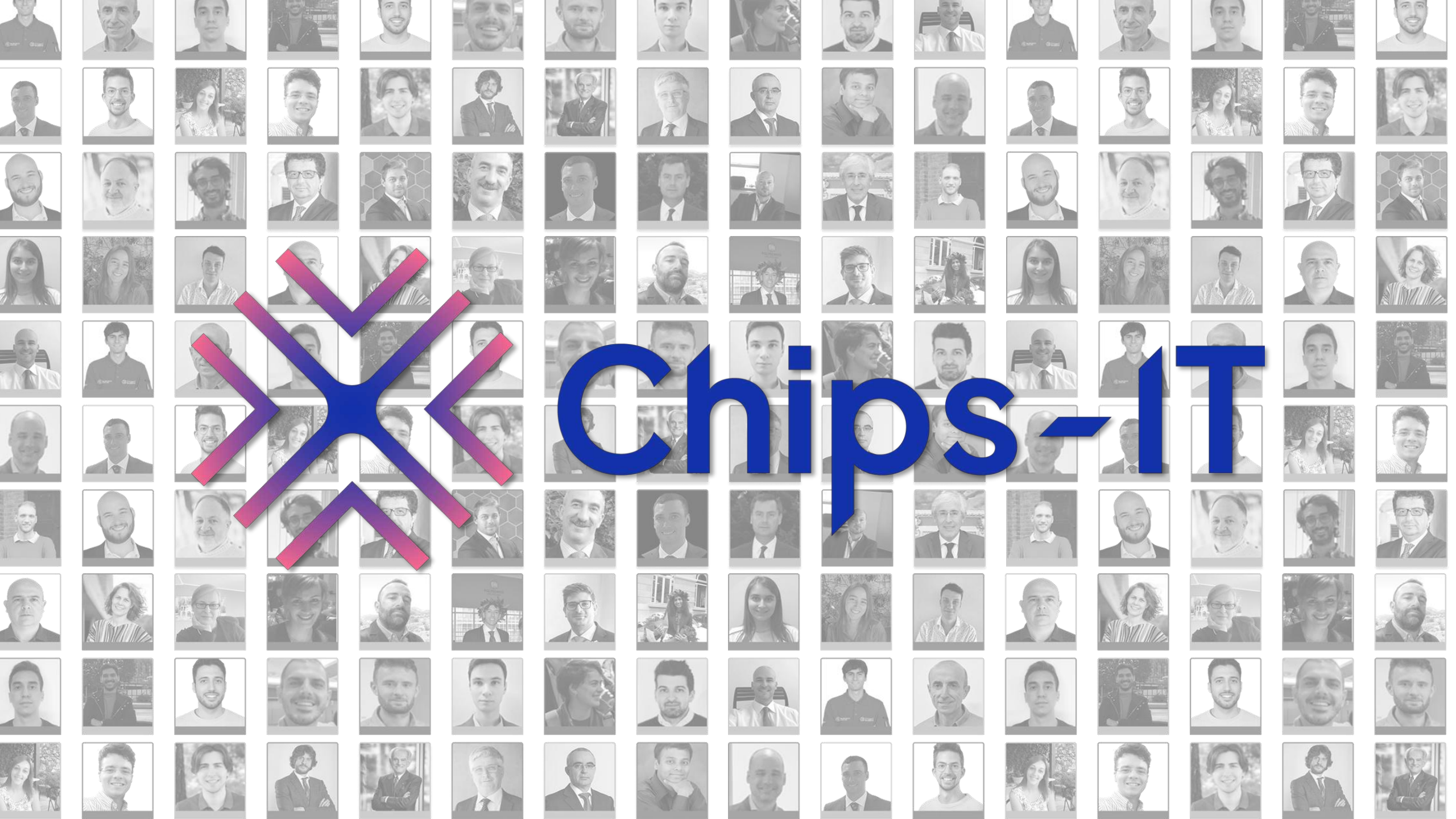
Early 2026
Full advanced RF testing lab 100-300GHz
7M€

Late 2026
Full advanced digital circuits testing and initial analog testing capability
13M€

2027
Added capability for digital and analog testing
2M€

Chips-IT aims :

- To make Italy and Europe a better place to do microelectronics with its R&D activity and partnerships
- To be the place where Italian ideas and ingenuity in advanced technology become economic growth and solutions to society problems.


Chips-IT